AI Chips Are Being Built in the Dark

The next frontier isn’t software—it’s the physics of chip packaging.

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THE DATA

TSMC Fab Expansion

This massive capital outlay underscores a fundamental shift: AI scalability is no longer driven by transistor count alone. Instead, the physical layer—co-packaged optics, 3D stacking, and system-on-package (SoP) architectures—is now the primary constraint. Without breakthroughs in packaging, even the most advanced logic nodes will underperform.



Source: forbes.com
https://www.forbes.com/sites/zinnialee/2026/11/05/this-nvidia-backed-ai-startup-is-helping-chip-giants-save-time-and-money/

01

Packaging Is the New Frontline

The shift from Moore’s Law to system-level integration means that the true innovation in AI chips is now happening in the interconnect layer. CoWoS and InFO packaging are no longer add-ons—they are the core of performance. This redefines where competitive advantage lies: not in the fab, but in the assembly and interconnect design.



02

Education Must Catch Up to Physics

As physical layer complexity rises, so does the talent gap. Carnegie Mellon's new CS Learn platform, offering free access to VLSI and digital logic courses, is not just a resource—it's a strategic response to a global shortage of engineers who understand chip-level integration. Without this workforce, even the most advanced fabs will sit idle.

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